REMARKS:

Applicants have carefully studied the Final Examiner's Action and all references cited therein. The amendment appearing above and these explanatory remarks are believed to be fully responsive to the Action. Accordingly, this important patent application is now believed to be in condition for allowance.

Applicants respond to the outstanding Action by centered headings that correspond to the centered headings employed by the Office, to ensure full response on the merits to each finding of the Office.

Claim Rejections – 35 U.S.C. § 103

Applicants acknowledge the quotation of 35 U.S.C § 103(a).

Claims 1-24 stand rejected under 35 U.S.C § 103(a) as being unpatentable over Applicants' Admitted Prior Art [hereinafter AAPA] in view of Park et al. [US 5,526,508 A; hereinafter Park].

Regarding independent claim 1, the Office states that the AAPA discloses a method for transferring information to a bus (i.e. Bus 106 of Fig. 1; See page 7, paragraph [0025], lines 1-3), comprising: receiving an indication (i.e. CPU_WR_COM or CPU_RD_COM) that information (i.e. CAD, CDW, and CCO in Fig. 2-3) is to be transferred to a bus (i.e. Bus 106 of Fig. 1; See page 8, paragraph [0028]); reading a bus grant indication (i.e., indication on GNT/PARKING-GNT in Fig. 2; See page 9, paragraph [0029]); writing the information (i.e., said CAD, CDW, and CCO) to a buffer (i.e. Two-Entry Buffer 202 of Fig. 2); and transferring the information (i.e., said information CAD, CDW, and CCO in said Two-Entry Buffer) to the bus if the bus grant indication (i.e., said GNT/PARKING-GNT) indicates that transfer of the information to the bus is allowed (see page 9, paragraph [0029]). Additionally, the Office states that the AAPA does not teach said writing the information to said buffer if the bus grant indication does not indicate that transfer of the information to the bus is allowed, and bypassing the buffer and said transferring the information to the bus if the buffer is empty and the transfer of the information to

the bus is allowed, but that Park discloses a method for a cache line replacing system (See Fig. 3 and Abstract), wherein said method (i.e., said method for cache line replacing system) for reducing latency in information transfers (See col. 3, lines 2-3) to a bus (i.e., CPU/Cache bus 31 of Fig. 3) including writing information (i.e., line of cache data) to a buffer (i.e., RD Buffer 36 of Fig. 3) if a bus grant indication does not indicate that transfer of the information to the bus is allowed (i.e., said CPU/Cache bus is not allowed to be used by memory read cycle during write back cycle of the steps 51 and 52 in Fig. 5, in other words, said CPU/Cache bus is occupied by said write back cycle; See col. 6, lines 11-14); and bypassing the buffer (See title; bypassing said RD buffer) and transferring the information (i.e., line of cache data) to a bus (i.e., said CPU/Cache bus) if a buffer (i.e., RD Buffer) is empty (i.e., said Buffer WT Reg counts 'zero'; See col. 5, lines 26-30) and transfer of the information to the bus is allowed (i.e., said CPU/Cache bus is allowed for memory read cycle after write back data having been stored in write-back buffer; See col. 3, lines 27-35, and col. 4, lines 31-46). Applicants respectfully disagree with the finding of the Office.

Claim 1 has been amended to more clearly describe that which the Applicants regard as the invention. Amended claim 1 includes the method step of, receiving an indication that information is to be transferred from a device to a bus in a first clock cycle and reading a bus grant indication in the first clock cycle. Support for the amendment can be found at paragraph [0042] of the specification as filed, which states that, "the status of the grant line (GNT/PARKING-GNT) is checked in the same clock cycle that the Control Logic **501** receives an indication from the CPU **101** that information is to be transferred to the Bus **106**". As such, the information to be transferred in the case of the present invention is immediately available for transfer from the CPU Bus **104** to the Bus **106** in the first clock cycle.

By contrast, as described in the Background of the Invention in reference to the Applicants' Admitted Prior Art, the prior art teaches at paragraph [0029] of the specification that information is transferred from the Buffer **202** to the Bus **106** in a first clock cycle after receiving a grant indication on a grant line and on the next clock cycle which follows the first writing of information to the Buffer **202**, the Control Logic **201** then checks to see if a parking grant (PARKING-GNT) is active on the grant line. As such, the AAPA teaches writing information to the buffer in a first clock cycle and then checking the status of the grant line in a subsequent

clock cycle. This is in contrast to the present invention which describes and claims receiving an indication that information is to be transferred from a device to a bus in a first clock cycle and reading a bus grant indication in the first clock cycle.

To establish a *prima facie* case of obviousness, the prior art cited must teach or suggest all the claim limitations. Neither the Park et al. reference nor the Applicants' Admitted Prior Art teach or suggest the step of receiving an indication that information is to be transferred from a device to a bus in a first clock cycle and reading a bus grant indication in the first clock cycle. Therefore, a *prima facie* case of obviousness has not been established because the cited references fail to disclose all the elements of the Applicants' invention.

Independent claim 9 has been amended to more clearly describe that which the Applicants regard as the invention. Amended claim 9 includes logic configured to receive an indication from the device in a first clock cycle that information is to be transferred to the bus, read a bus grant indication in the first clock cycle, and cause the information to either be stored in the buffer if the bus grant information does not indicate that transfer of the information from the device to the bus is allowed, or be transferred from the device to the bus, thereby bypassing the buffer, if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed. For the reasons cited with regard to independent claim 1, as applied to amended independent claim 9, neither the Park et al. reference nor the Applicants' Admitted Prior Art teach or suggest logic configured to receive an indication from the device in a first clock cycle that information is to be transferred to the bus, read a bus grant indication in the first clock cycle, and cause the information to either be stored in the buffer if the bus grant information does not indicate that transfer of the information from the device to the bus is allowed, or be transferred from the device to the bus, thereby bypassing the buffer, if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed as described and claimed by the present invention. Therefore, a *prima facie* case of obviousness has not been established because the cited references fail to disclose all the elements of the Applicants' invention.

Independent claim 19 has been amended to more clearly describe that which the Applicants regard as the invention. Amended claim 19 includes logic configured to receive an indication from a device in a first clock cycle that information is to be transferred to the bus, read a bus

grant indication in the first clock cycle, and provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus grant indication indicates that the bus is available for transfer of the information to the bus. For the reasons cited with regard to independent claim 1, as applied to amended independent claim 19, neither the Park et al. reference nor the Applicants' Admitted Prior Art teach or suggest logic configured to receive an indication from the device in a first clock cycle that information is to be transferred to the bus, read a bus grant indication in the first clock cycle, and provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus grant indication indicates that the bus is available for transfer of the information to the bus as described and claimed by the present invention. Therefore, a *prima facie* case of obviousness has not been established because the cited references fail to disclose all the elements of the Applicants' invention.

For the reasons cited above, Applicants believe that amended independent claim 1 is patentable over Applicants' Admitted Prior Art in view of Park et al. and is believed to be in condition for allowance.

Claims 2-8 are dependent upon claim 1, and are therefore allowable as a matter of law.

For the reasons cited above, Applicants believe that amended independent claim 9 is patentable over Applicants' Admitted Prior Art in view of Park et al. and is believed to be in condition for allowance.

Claims 10-18 are dependent upon claim 9, and are therefore allowable as a matter of law.

For the reasons cited above, Applicants believe that amended independent claim 19 is patentable over Applicants' Admitted Prior Art in view of Park et al. and is believed to be in condition for allowance.

Claims 20-24 are dependent upon claim 19, and are therefore allowable as a matter of law.

If the Office is not fully persuaded as to the merits of Applicant's position, or if an Examiner's Amendment would place the pending claims in condition for allowance, a telephone call to the undersigned is requested.

Respectfully Submitted,

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Date

\Kenneth Glass\
Kenneth Glass
Attorney for Applicants
Reg. No. 42587

Kenneth Glass
PO Box 1220
Los Gatos, CA 95031-1220
Tel. (408) 354-4448